

Reg. No:

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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech I Year II Semester Regular Examinations November-2021

DIGITAL LOGIC DESIGN

(Common to CSE (AI & ML) & CSE (IoT & CS Including BCT))

Time: 3 hours

Max. Marks: 60

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

- 1 a Convert the following numbers L5 3M
 i) $(AB)_{16} = ()_2$ ii) $(1234)_8 = ()_{16}$ iii) $(101110.01)_2 = ()_8$
 b Convert the following to binary and then to gray code $(AB33)_{16}$ L5 4M
 c Perform the following Using BCD arithmetic $(7129)_{10} + (7711)_{10}$ L5 5M

OR

- 2 Prove the following identities:
 a $A' B' C' + A' B C' + A B' C' + A B C' = C'$ L5 6M
 b $A B + A B C + A' B + A B' C = B + A C$ L5 6M

UNIT-II

- 3 Simplify the following Boolean expression using K-MAP and implement using NAND gates. $F(W,X,Y,Z) = XYZ + WXY + WYZ + WXZ$ L6 12M
 OR
 4 Simplify the following expressions, and implement them with two-level NAND gate circuits:
 i) $AB' + ABD + ABD' + A'C'D' + A'BC'$ L6 12M
 ii) $BD + BCD' + AB'C'D'$

UNIT-III

- 5 Draw and explain the working of a Carry- Look ahead adder? L2 12M
 OR
 6 a Implement the following Boolean function using 8:1 multiplexer L5 6M
 $F(A,B,C,D) = \sum m(0,1,2,5,7,8,9,14,15)$
 b Explain Full binary subtractor in detail? L2 6M

UNIT-IV

- 7 Explain the working of the following L2 12M
 i) J-K flip-flop ii) S- R flip-flop iii) D flip-flop
 OR
 8 What is race-around condition? How its elimination does is a Master-slave J-K flip-flop? L1 12M

UNIT-V

- 9 Implement the following functions using PLA. L5 12M
 $A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$ $C(x,y,z) = \sum m(2,6)$
 OR
 10 Explain about Error correction & Detection Codes with examples? L2 12M

*** END ***